

Cryogenic silicon surface ion trap

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Abstract. Trapped ions are pre-eminent candidates for building quantum information processors and quantum simulators. They have been used to demonstrate quantum gates and algorithms, quantum error correction, and basic quantum simulations. However, to realise the full potential of such systems and make scalable trapped-ion quantum computing a reality, there exist a number of practical problems which must be solved. These include tackling the observed high ion-heating rates and creating scalable trap structures which can be simply and reliably produced. Here, we report on cryogenically operated silicon ion traps which can be rapidly and easily fabricated using standard semiconductor technologies. Single $^{40}\text{Ca}^+$ ions have been trapped and used to characterize the trap operation. Long ion lifetimes were observed with the traps exhibiting heating rates as low as $\dot{\bar{n}} = 0.33$ phonons/s at an ion-electrode distance of $230\text{ }\mu\text{m}$. These results open many new avenues to arrays of micro-fabricated ion traps.

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1. Introduction

Processing information using a quantum system allows problems to be solved which are difficult or impossible to compute classically [1], and trapped atomic ions provide a promising platform for such quantum information processors [2, 3, 4]. Ions can be confined using a combination of radio-frequency (RF) and static (DC) electric fields [5]. The electrode structures required to create the appropriate fields can take a variety of geometries, and great progress has recently been made using planar structures [6, 7]. For these, all electrodes are located in a plane above which the ions are trapped. Notable among the advantages of such a structure is the scalability: arrays with hundreds or thousands of traps can in principle be built on a single chip using very-large-scale integration (VLSI) technologies like optical lithography and etching [8], far exceeding what is possible using bulk fabrication.

In making such traps a reality, a number of features must be considered. It is essential that scalable trap architectures have low RF losses: if the losses are too high the RF voltage applied in order to trap will be dissipated in the chip. Beyond this, microfabrication has become highly developed and it would be desirable to bring these techniques to bear on ion traps. For large arrays of traps the creation of through-wafer vias [9], so that electrical connections can be made throughout the array, is a prerequisite. Optical addressing of ions in an array can be facilitated by fabrication of holes through the substrate. Moreover, the integration of on-chip electronics, such as would be afforded by CMOS (Complementary Metal-Oxide-Semiconductors), would open up untold possibilities for ion traps.

Surface ion traps can be broadly divided into two groups, according to the type of substrate material: dielectric or semiconductor. Dielectric substrates like sapphire or fused silica have a very low RF power dissipation. For such traps the electrodes are created by simple optical lithography combined with lift-off processes or electroplating on top of the substrate [10]. However, dielectric materials are difficult to pattern by means of wet or dry etching and not suitable for features such as through-wafer vias. The second type of substrate materials are semiconductors, such as silicon, which are easy to structure. Slots, holes and vias with aspect ratios up to 160 can be etched by standard techniques [11]. However, the RF power dissipation is significant and therefore a ground electrode is required to shield the substrate from RF fields. This in turn necessitates a more complicated fabrication process and precludes vias for RF electrodes [12, 13].

In this paper, we report on a new silicon surface ion trap built for cryogenic applications. The design permits the use of standard silicon processing techniques, while mitigating the problems of RF loss: silicon becomes an insulator at low temperature and consequently the RF loss decreases by several orders of magnitude [14]. This obviates the need for a shielding electrode and so simplifies the trap design. The cryogenic environment inheres several additional advantages. Ultra-high vacuum can be attained within a few hours due to cryogenic pumping, without baking the system [15]. This facilitates fast turn-around times for trap installation (~ 1 day). Furthermore, operation

at liquid-helium temperatures reduces the rate at which the ions' motion is heated, typically by around two orders of magnitude [16]. This is beneficial as it increases the coherence time of the ions' motion, which is used to transfer quantum information between different ions.

2. Trap design and fabrication

The planar design used for this work is illustrated in figure 1. To fabricate the traps an undoped silicon substrate is patterned by optical lithography and deep reactive ion etching (see figure 2(b)).

Deep undercut trenches are etched in the substrate and mark the gaps between the individual electrodes. Following a thermal growth of $2\text{ }\mu\text{m}$ of SiO_2 the electrodes are formed by evaporation of gold perpendicular to the surface. Due to the undercuts, there is no electrical connection between the different electrodes (figure 1(b), 2(b)) and no further lift-off or etching steps are necessary. There are no further cleaning steps and, to avoid any contamination of the surface, the gold electrodes are never brought into contact with liquids such as solvents for cleaning. The fabrication process and the packaging are explained in detail in Appendix A.1.

Ions are trapped $230\text{ }\mu\text{m}$ above the centre electrode by applying an RF voltage to the two RF electrodes. Lasers used to Doppler cool the ions are aligned parallel to the plane of the trap, to minimise scatter from the surface. To efficiently cool the ions along all three principal axes of their motion, each axis must have a projection along the direction of the cooling laser beam. Consequently, none of the principal axes of motion should be perpendicular to the trap surface. The RF electrodes have thus been fabricated with unequal widths ensuring that the two radial principal axes both have a component parallel to the trap surface [17]. Seven segmented electrodes are located on each side of the two RF electrodes. DC voltages are applied to these electrodes and create confinement along the axial (z) direction. Ions can be shuttled along the z -axis by changing the DC voltages. Stray electric fields arising from contamination of the trap or imperfection in trap fabrication can cause micromotion [18], which is minimised by adding suitable DC voltages to the segmented DC electrodes.

Initially, the operation of a single trap (trap #1) was characterised in detail over several weeks. To demonstrate the reproducibility of the results, a further five traps from two different silicon wafers were tested, and shown to exhibit similar behaviour.

3. Cryogenic setup

The silicon ion trap is cooled to 10 K in a closed-cycle, two-stage, Gifford McMahon cryostat equipped with a vibration-isolation system [19, 15] to reduce the vibrations at the trap to around 100 nm at 2 Hz. The trap is attached to the second cooling stage of the cryostat (figure 2(a)). It is enclosed by a copper shield, also cooled to 10 K. This minimises the incident black-body radiation and reduces the number of background

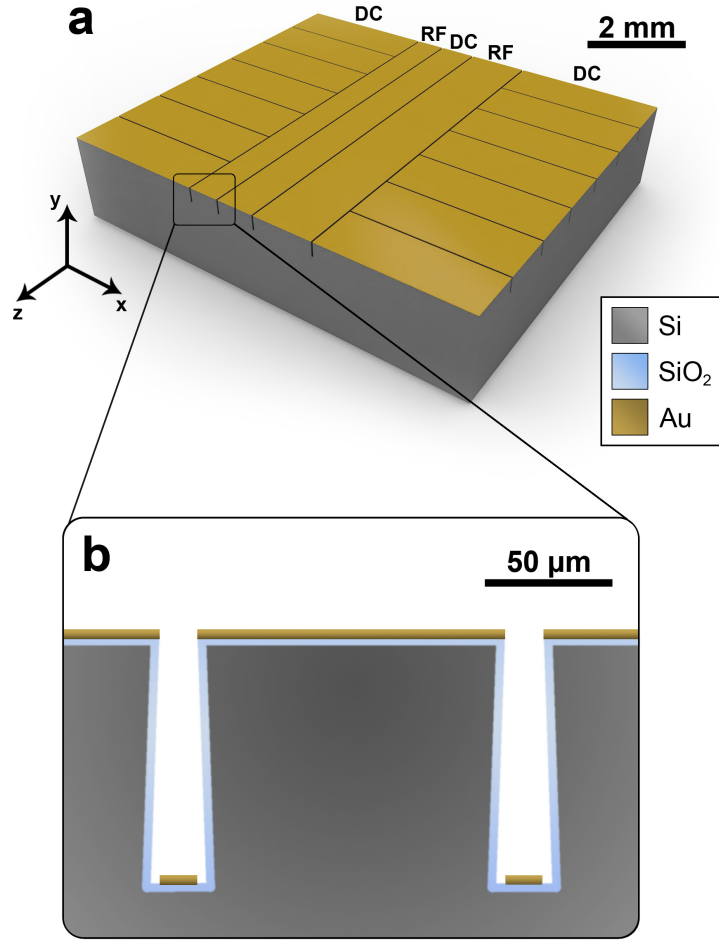


Figure 1. (a) Schematic showing the surface-trap design. The trap consists of a pair of asymmetric RF electrodes (widths of $200\ \mu\text{m}$ and $400\ \mu\text{m}$ respectively), a centre DC electrode (width: $250\ \mu\text{m}$) and seven segmented DC electrodes on each side (axial width: $350\ \mu\text{m}$). The electrode separation is $10\ \mu\text{m}$. This geometry allows strings of ions to be trapped $230\ \mu\text{m}$ above the surface. (b) Cross section through the trap. Trenches etched to a depth of $\sim 100\ \mu\text{m}$ separate the individual electrodes. The entire silicon surface is covered by a thermally grown SiO_2 layer preventing metals from diffusing into the silicon. The trap electrodes are created by gold deposition normal to the surface. Well-defined undercuts prevent electrical connection between the different electrodes.

molecules at the trapping site, as they freeze on the shield walls. To reduce surface contamination caused by molecules freezing out on the trap electrodes during the cool down, the second stage of the cryostat is kept at $320\ \text{K}$ till the first stage has reached a temperature of $240\ \text{K}$. Thereafter the second stage is cooled to $10\ \text{K}$, while the first stage reaches a final temperature of $50\ \text{K}$. $^{40}\text{Ca}^+$ ions are loaded from a neutral Ca-beam produced by a resistively heated oven located within the vacuum chamber but not mechanically connected to the cold stage. The atoms are introduced to the trapping region through a small hole in the copper shield (diameter $\sim 3\ \text{mm}$) and are ionized by

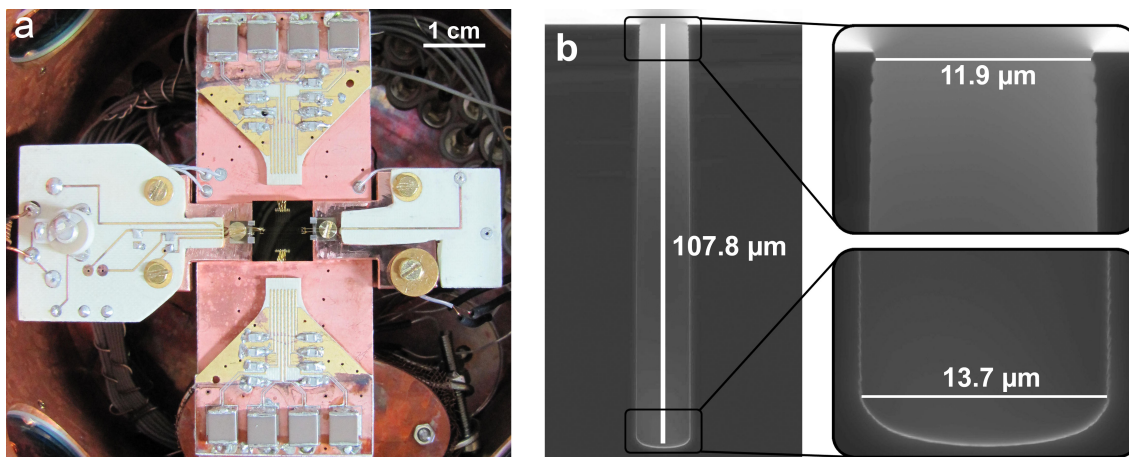


Figure 2. (a) Cryostat's 10K stage. The trap is at the centre. The DC filters are located on the vertical printed circuit board. The LC drive circuit is mounted on the left of the trap and a capacitive divider for measuring the trap voltage is on the right. (b) Scanning electron microscope images of an undercut trench formed by deep reactive ion etching separating two electrodes.

a two-photon process [20] in the trapping region.

The voltage on the RF electrodes (amplitude $U_0 = 140$ V, frequency $\Omega_T/2\pi = 20.6$ MHz) is provided by an LC lumped-circuit resonator driven by a function generator [19] and creates a trapping potential with trap depth of 75 meV. The power dissipation in the resonator goes as $P_D = U_0^2 C \Omega_T / 2Q$, where C is the resonator capacitance and Q the quality factor of the resonator. To keep P_D low, C must be kept small. This can be achieved by locating the resonator in vacuum next to the trap on the cold stage of the cryostat (see figure 2(a)). This reduces C to 9.5 pF, which is mainly limited by the capacitance of the RF electrodes. The power necessary for trapping is less than 10 mW, which is well below the cryostat's cooling power of 500 mW and increases the temperature measured next to the trap by only 0.2 K. Filters with a cut-off frequency of 4.8 kHz are mounted on the cold stage next to the resonator in order to filter the voltages applied to the DC electrodes (see Appendix A.2 for further details on the LC resonator and DC filters).

4. Silicon at cryogenic temperatures

Intrinsic silicon is already used for several superconducting-qubit applications in the mK-range [21, 22]. In contrast, all silicon-based ion traps to date have been designed for room-temperature operation. In some cases, the issue of RF losses was mitigated by using highly doped silicon for the trap electrodes [23, 24] or substrate [25]. This method would not, however, work in a cryogenic environment because of the silicon's low electrical conductivity at low temperatures. In other cases there was an additional ground electrode which shielded the silicon against the trapping RF voltage [12, 13]. At low temperature the charge carriers in intrinsic silicon freeze out, leaving the substrate as

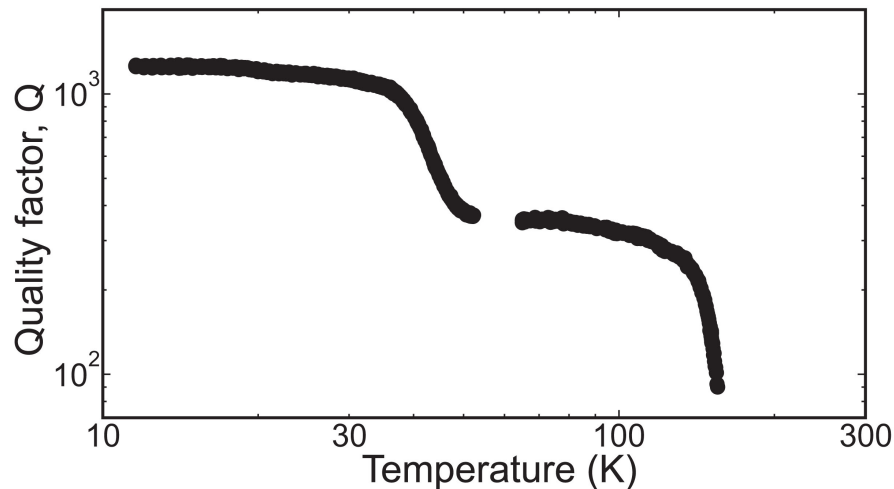


Figure 3. Resonator quality factor as a function of temperature. The inductive and capacitive parts of the LC resonator are predominantly provided by a copper air-coil and the trap RF electrodes, respectively. At room temperature, the entire RF driving power is absorbed by the silicon substrate and there is no measurable resonance. On cooling, the conductivity of the inductor increases (thereby increasing its quality factor, Q_L). Cooling also reduces the charge-carrier concentration in the silicon and, below 100 K, causes a steep decrease of its electrical conductivity and loss tangent (thereby increasing the capacitive quality factor, Q_C). These effects all serve to increase the overall Q , with the plateau around 100 K being due to the non-linear response of the material properties. Below 20 K, the quality factor is comparable to that measured with a fused-silica trap, meaning that Q is limited by Q_L and that $Q_C \gg Q_L$. The data shown were measured in trap #1 (cf. table 1). The other five traps tested showed similar behaviour.

a good insulator with low RF loss. This obviates the need for a shielding electrode, which in turn reduces the trap capacitance and the power dissipation, as well as permitting a range of new fabrication techniques.

The traps presented here are especially built for low-temperature applications. The characterisation of the RF resonator (including the trap) as a function of temperature is shown in figure 3. The inductor of the LC resonator is provided by a copper coil with an air (vacuum) core and the capacitance primarily comes from the trap RF electrodes. The quality factor, Q , was recorded while the cryostat was slowly heated up. The temperature was measured by a silicon diode mounted on the copper trap carrier. Q follows the relation $1/Q = 1/Q_L + 1/Q_C$, where Q_L and Q_C are the quality factors of the inductor and the capacitor, respectively.

At room temperature the silicon substrate, which supports the RF electrodes, has a very high loss tangent [14], $\tan \delta$, of 1.5 at the driving frequency $\Omega_T/2\pi = 20.6$ MHz. For comparison [26], under the same conditions, $\tan \delta$ of fused silica is around $\sim 10^{-4}$. Due to the high loss tangent, at room temperature the entire RF driving power is absorbed by the silicon substrate. There is no measurable resonance: using an impedance analyser the resonator Q was indistinguishable from zero. In contrast, a quality factor of 400

was measured in a similar trap fabricated on a fused-silica substrate and operated at room temperature. Cooling leads to a reduction of the charge-carrier concentration in the silicon and, below 100 K, to a steep decrease of the electrical conductivity and loss tangent. Ultimately, electron-hole pairs freeze out at ~ 25 K and the silicon becomes an insulator [14]. In addition to these changes in the silicon, the electrical conductivity of the coil increases with decreasing temperature, and therefore the inductor quality factor, Q_L , goes up [19]. Increasing Q_C and Q_L leads to an increasing overall resonator quality factor, Q , with decreasing temperature, as shown in figure 3. Below 20 K the value of $Q > 1200$ is comparable to that measured with a fused-silica trap at the same temperature indicating that Q is then only limited by Q_L and not by RF absorption in the silicon.

5. Trapped ion lifetime

A trapping parameter which becomes especially important with a large number of trapped ions is the length of time for which an ion can be trapped, sometimes called the trapped-ion lifetime. Assuming a mean lifetime of 1 hour, which follows an exponential decay, a trap array holding 1000 ions would lose ions at a rate of around one per second. Ions are usually lost by collisions with background gas molecules or by motional heating. A cryogenic setup is an ideal tool to achieve long lifetimes since it provides extremely high vacuum and helps to reduce heating rates [15, 16].

In trap #1, ion lifetimes of up to 9 hours were observed without laser cooling. With laser cooling, no ion losses were recorded over a total experimental period of more than 50 hours with a single ion. The trap is therefore suitable for scaling up to hundreds of ions without the need for continuous reloading. Five further traps were tested for shorter periods and the results from these traps were consistent with the more extended observations made with trap #1.

6. Heating rates

For many quantum-information applications ions should be at or near their motional ground state, and heating of the ions' motion degrades the quality of quantum operations. Trapped ions are predominately heated by electric-field noise resonant with the ions' motional frequencies. To measure the heating rate [27], the axial motion of a single ion was cooled to near the ground state by resolved-sideband cooling. Following a predefined waiting time, the mean phonon number was determined by two different methods: measurement of the transition probability on the red and blue sidebands and Rabi flops on the blue sideband [27]. The heating rate was determined by the change in phonon number with different waiting times (figure 4).

Over a period of six weeks, the heating rate in trap #1 was measured several times and found to be constant, within the error bars, at $\dot{n} = 0.6(2)$ phonons/s. The electric-field noise inferred to underlie this heating [16] is $S_E = 4.4 \times 10^{-15} \text{ V}^2 \text{ m}^{-2} \text{ Hz}^{-1}$. Heating

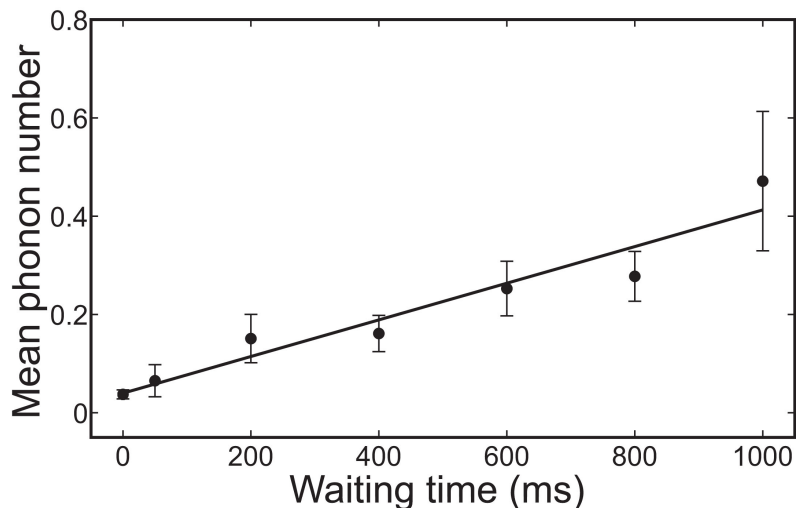


Figure 4. Heating-rate measurement. Mean phonon number \bar{n} of the axial mode ($\omega_z/2\pi = 1.069$ MHz) as a function of the waiting time after ground state cooling. \bar{n} was determined by measuring the Rabi flops on the blue sideband [27]. In this instance the heating rate, taken to be the gradient of a linear fit to the data, is $\dot{\bar{n}} = 0.37(6)$ phonons/s. Taking data on different days over a period of six weeks the trap exhibited a heating rate of $\dot{\bar{n}} = 0.6(2)$ phonons/s.

Table 1. Heating rates of different Si traps. Heating rates of six traps, all of the same design, with an ion-electrode separation of $230\ \mu\text{m}$. Measurements were made over 84 days. Traps #1-5 were taken from a single Si wafer, with trap #6 being from a second wafer. The heating rate measured in trap #5 is $0.33(4)$ phonons/s, which is the lowest rate ever reported.

Trap #	Heating rate (phonons/s)	Axial freq. (MHz)
1	0.6(2)	1.069
2	3.3(2)	1.059
3	0.96(7)	1.069
4	0.95(7)	1.045
5	0.33(4)	1.066
6	21.5(8)	1.073

rates were measured in five further traps, four from the same wafer and one (trap #6) from a second wafer, with the results given in table 1.

Trap #5 exhibits a heating rate of $0.33(4)$ phonons/s, which is the lowest rate ever reported: the lowest previously-reported heating rates are $0.83(10)$ phonons/s at room temperature, in a trap with a $3.5\ \text{mm}$ ion-electrode separation [28], and $2.1(3)$ phonons/s at cryogenic temperatures in an trap with a $100\ \mu\text{m}$ ion-electrode separation [29]. Trap #6 exhibits a heating rate of $21.5(8)$ phonons/s. This falls well within the range of heating rates observed in other cryogenic ion traps [16, 30], but is significantly higher than the other five traps tested here. The second wafer, from which trap #6 was taken, was patterned separately from the first, using slightly modified etch parameters. It is

conjectured that this may be the reason for the higher heating rate.

7. Conclusion

We have presented a new ion-trap design based on a silicon substrate. This will allow trap fabrication to benefit from well-developed silicon-fabrication processes. The design was made possible by exploiting the fact that, at low temperatures, silicon becomes an insulator with low RF losses. The traps exhibit a high Q and reproducibly low ion-heating rates. Fabrication can be easily extended to include slots for increased optical access and through-wafer vias. Unlike room-temperature silicon traps, vias in our design would also work at RF frequencies, allowing the realization of a 2D trap array with adjustable RF electrodes [31]. Heating-rate and lifetime measurements indicate that a trap array based on our design with several hundred sites should be practicable. Moreover, one might ultimately envision such trap arrays integrated with a wide variety of other silicon-based technologies including CMOS electronics, micro-optics, micro- and nano-mechanical systems, and sensors. This would ultimately mean that the entire science package, including optical, mechanical, and electronic functions could be integrated on a single substrate to provide a quantum lab on a chip.

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Appendix A.

Appendix A.1. Trap fabrication and packaging

High-purity float-zone silicon wafers (diameter: 100 mm, thickness: $525\ \mu\text{m}$) with specific resistivity larger than $5000\ \Omega\text{cm}$ were used. The wafers were coated by the positive photoresist AZ1518 with a thickness of $2.4\ \mu\text{m}$. The resist was patterned by means of standard optical lithography. The wafers were deep reactive ion etched by gas chopping based on SF_6 and C_4F_8 to create trenches with slight undercuts separating the different electrodes of the ion traps. The $10\ \mu\text{m}$ gaps between the electrodes were etched to a depth of $\sim 100\ \mu\text{m}$ with an undercut of $\sim 1\ \mu\text{m}$. The resist was then removed by O_2 plasma cleaning. A $2\ \mu\text{m}$ thick SiO_2 layer was grown on the silicon surface by thermal oxidation to prevent metals from diffusing into the silicon. Each wafer provided 52 traps and the individual trap chips were separated by laser scribing. To form the electrodes, titanium and gold layers of a thickness of 2 nm and 500 nm respectively were deposited on the substrate surface by electron-beam evaporation. No further cleaning steps were performed after evaporation.

Traps were mounted on a copper carrier. To ensure good thermal contact between the trap and the carrier, each trap was coated on the backside with a thin layer of heat-conducting grease and then clamped in place by two stainless-steel forks. Printed circuit boards (PCBs) supporting the DC filters and the LC resonator were glued to the carrier. The trap electrodes were connected to the PCBs by $25\ \mu\text{m}$ thick gold wirebonds. The copper traces on the PCBs were partially gold-electroplated to increase the adhesion of the bonding wires. The entire fabrication and assembly process took place in a cleanroom to reduce surface contamination. The only exception to this was installing the trap in the cryostat itself which was not located in a cleanroom, though this step took less than ten minutes.

Appendix A.2. LC resonator and DC filter

The lumped-circuit LC resonator is similar to that reported by Gandolfi et al.[19] and is formed by a copper air-coil inductor with an inductance of $6.3\ \mu\text{H}$ mounted next to the trap, a capacitance of $9.5\ \text{pF}$ provided by the trap's RF electrodes, and a capacitive voltage divider. The circuit's resonance frequency is 20.6 MHz at 10 K. The capacitive divider, which allows the measurement of the voltage on the RF electrodes, has a ratio of 1:400 and a total capacitance of $2.5\ \text{pF}$. Furthermore, there is a matching network to match the LC circuit to $50\ \Omega$. This consists of a tunable capacitor ($12\text{--}100\ \text{pF}$) and an inductor ($186\ \text{nH}$) connected in series and parallel, respectively.

For best trapping performance all DC electrodes must be properly RF-grounded which can be accomplished by installing capacitors as close as possible to the DC electrodes. For this reason, small surface-mounted NP0 capacitors with a capacitance of $470\ \text{pF}$ are located $\sim 15\ \text{mm}$ from the electrodes. Additionally, RC low-pass filters are used to filter RF noise on the DC lines. The filters each consist of a $100\ \Omega$ thin-film

resistor and a 330 nF NP0 capacitor placed ~ 30 mm from the trap. The cut-off frequency of these filters is 4.8 kHz. The resistors and capacitors used are cryo-compatible and do not significantly change performance during cooling. In addition to these filters there are 6th-order RC low-pass filters outside of the vacuum chamber with a cut-off frequency of 80 Hz.

References

- [1] Michael A. Nielsen and Isaac L. Chuang. *Quantum Computation and Quantum Information*. Cambridge University Press, 2011.
- [2] T. D. Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien. Quantum computers. *Nature*, 464:45–53, 2010.
- [3] Rainer Blatt and David Wineland. Entangled states of trapped atomic ions. *Nature*, 453:1008–1015, 2008.
- [4] P. Zoller, Th. Beth, D. Binosi, R. Blatt, H. Briegel, D. Bruss, T. Calarco, J. I. Cirac, D. Deutsch, J. Eisert, A. Ekert, C. Fabre, N. Gisin, P. Grangiere, M. Grass, S. Haroche, A. Imamoglu, A. Karlson, J. Kempe, L. Kouwenhoven, S. Kröll, G. Leuchs, M. Lewenstein, D. Loss, N. Lütkenhaus, S. Massar, J. E. Mooij, M. B. Plenio, E. Polzik, S. Popescu, G. Rempe, A. Sergienko, D. Suter, J. Twamley, G. Wendin, R. Werner, A. Winter, J. Wrachtrup, , and A. Zeilinger. Quantum information processing and communication strategic report on current status, visions and goals for research in europe. *Eur. Phys. J. D*, 36:203–228, 2005.
- [5] F. G. Major, Viorica N. Gheorghe, and Gunther Werth. *Charged Particle Traps: Physics and Techniques of Charged Particle Field Confinement*. Springer, 2005.
- [6] J. Chiaverini, R. B. Blakestad, J. Britton, J. D. Jost, C. Langer, D. Leibfried, R. Ozeri, and D. J. Wineland. Surface-electrode architecture for ion trap quantum information processing. *Quantum Inf. Comput.*, 5:419, 2005.
- [7] Marcus D. Hughes, Bjoern Lekitsch, Jiddu A. Broersma, and Winfried K. Hensinger. Microfabricated ion traps. *Contemp. Phys.*, 52(6):505–529, 2011.
- [8] J. Kim, S. Pau, Z. Ma, H.R. McLellan, J.V. Gates, A. Kornblit, R.E. Slusher, R.M. Jopson, I. Kang, and M. Dinu. System design for large-scale ion trap quantum information processor. *Quantum Inf. Comput.*, 5:515–537, 2005.
- [9] M. Motoyoshi. Through-silicon via (tsv). *Proc. IEEE*, 97(1):43–48, 2009.
- [10] S. Seidelin, J. Chiaverini, R. Reichle, J. J. Bollinger, D. Leibfried, J. Britton, J. H. Wesenberg, R. B. Blakestad, R. J. Epstein, D. B. Hume, W. M. Itano, J. D. Jost, C. Langer, R. Ozeri, N. Shiga, and D. J. Wineland. Microfabricated surface-electrode ion trap for scalable quantum information processing. *Phys. Rev. Lett.*, 96:253003, 2006.
- [11] Jayalakshmi Parasuraman, Anand Summanwar, Frdric Marty, Philippe Basset, Dan E. Angelescu, and Tarik Bourouina. Deep reactive ion etching of sub-micrometer trenches with ultra high aspect ratio. *Microelectron. Eng.*, 113(0):35–39, 2014.
- [12] D. T. C. Allcock, T. P. Harty, H. A. Janacek, N. M. Linke, C. J. Ballance, A. M. Steane, D. M. Lucas, Jr. Jarecki, R. L., S. D. Habermehl, M. G. Blain, D. Stick, and D. L. Moehring. Heating rate and electrode charging measurements in a scalable, microfabricated, surface-electrode ion trap. *Appl. Phys. B*, 107(4):913–919, 2012.
- [13] S Charles Doret, Jason M Amini, Kenneth Wright, Curtis Volin, Tyler Killian, Arkadas Ozakin, Douglas Denison, Harley Hayden, C-S Pai, Richart E Slusher, and Alexa W Harter. Controlling trapping potentials and stray electric fields in a microfabricated ion trap through design and compensation. *New J. Phys.*, 14:073012, 2012.
- [14] Jerzy Krupka, Jonathan Breeze, Anthony Centeno, Neil Alford, Thomas Claussen, and Leif Jensen. Measurements of permittivity, dielectric loss tangent, and resistivity of float-zone silicon at microwave frequencies. *IEEE Trans. Microw. Theory Techn.*, 54(11):3995–4001, 2006.

- [15] P. B. Antohi, D. Schuster, G. M. Akselrod, J. Labaziewicz, Y. Ge, Z. Lin, W. S. Bakr, and I. L. Chuang. Cryogenic ion trapping systems with surface-electrode traps. *Rev. Sci. Instrum.*, 80:013103, 2009.
- [16] Jaroslaw Labaziewicz, Yufei Ge, David R. Leibbrandt, Shannon X. Wang, Ruth Shewmon, and Isaac L. Chuang. Temperature dependence of electric field noise above gold surfaces. *Phys. Rev. Lett.*, 101:180602, 2008.
- [17] Fayaz A. Shaikh and Arkadas Ozakin. Stability analysis of ion motion in asymmetric planar ion traps. *J. Appl. Phys.*, 112:074904, 2012.
- [18] D. J. Berkeland, J. D. Miller, J. C. Bergquist, W. M. Itano, and D. J. Wineland. Minimization of ion micromotion in a Paul trap. *J. Appl. Phys.*, 83(10):5025–5033, 1998.
- [19] D. Gandolfi, M. Niedermayr, M. Kumph, M. Brownnutt, and R. Blatt. Compact radio-frequency resonator for cryogenic ion traps. *Rev. Sci. Instrum.*, 83:84705, 2012.
- [20] S. Gulde, D. Rotter, P. Barton, F. Schmidt-Kaler, R. Blatt, and W. Hogervorst. Simple and efficient photo-ionization loading of ions for precision ion-trapping experiments. *Appl. Phys. B*, 73:861–863, 2001.
- [21] Josephine B. Chang, Michael R. Vissers, Antonio D. Crcoles, Martin Sandberg, Jiansong Gao, David W. Abraham, Jerry M. Chow, Jay M. Gambetta, Mary Beth Rothwell, George A. Keefe, Matthias Steffen, and David P. Pappas. Improved superconducting qubit coherence using titanium nitride. *Appl. Phys. Lett.*, 103:012602, 2013.
- [22] J. E. Johnson, C. Macklin, D. H. Slichter, R. Vijay, E. B. Weingarten, John Clarke, and I. Siddiqi. Heralded state preparation in a superconducting qubit. *Phys. Rev. Lett.*, 109:050506, Aug 2012.
- [23] R. C. Sterling, H. Rattanasonti, S. Weidt, P. Srinivasan K. Lake, S. C. Webster, M. Kraft, and W. K. Hensinger. Two-dimensional ion trap lattice on a microchip. *arXiv:1302.3781 [quant-ph]*, 2013.
- [24] J. Britton, D. Leibfried, J. A. Beall, R. B. Blakestad, J. H. Wesenberg, and D. J. Wineland. Scalable arrays of RF Paul traps in degenerate Si. *Appl. Phys. Lett.*, 95:173102, 2009.
- [25] Guido Wilpers, Patrick See, Patrick Gill, and Alastair G. Sinclair. A monolithic array of three-dimensional ion traps fabricated with conventional semiconductor technology. *Nature Nanotech.*, 7:572–576, 2012.
- [26] George William C. Kaye and T.H. Laby. *Tables of Physical and Chemical Constants, Section 2.6.5 Dielectric properties of materials*. Longman, 1995.
- [27] D. Leibfried, R. Blatt, C. Monroe, and D. Wineland. Quantum dynamics of single trapped ions. *Rev. Mod. Phys.*, 75:281–324, Mar 2003.
- [28] G. Poulsen, Y. Miroshnychenko, and M. Drewsen. Efficient ground-state cooling of an ion in a large room-temperature linear paul trap with a sub-hertz heating rate. *Phys. Rev. A*, 86:051402, 2012.
- [29] S.X. Wang, Yufei Ge, Jaroslaw Labaziewicz, E. Dauler, Karl Berggren, and I.L. Chuang. Superconducting microfabricated ion traps. *Appl. Phys. Lett.*, 97(24):244102–244102–3, 2010.
- [30] Jaroslaw Labaziewicz, Yufei Ge, Paul Antohi, David R. Leibbrandt, Kenneth R. Brown, and Isaac L. Chuang. Suppression of heating rates in cryogenic surface-electrode ion traps. *Phys. Rev. Lett.*, 100:013001, 2008.
- [31] Muir Kumph, Michael Brownnutt, and Rainer Blatt. Two-dimensional arrays of radio-frequency ion traps with addressable interactions. *New J. Phys.*, 13(7):073043, 2011.